

## FACSIMILE COVER PAGE

**To :** USPTO: Formal NEW

**From :** Chris Rode

**Sent :** 11/18/04 at 2:13:40 AM

**Pages :** 8 (including Cover)

**Subject :** IDS after Final Office Action for pending application 09/287,478

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**NOV 18 2004**

United States Patent and Trademark Office  
Washington, D.C. 20231  
11/17/2004

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Dear Sir / Madam:

Please find attached an information disclosure, PTO/SB/08a, with requisite statement and fee for pending application 09/287,478 per 37CFR1.97(d)(1) and 37CFR1.97(e)(2) for an application having received a final office action.

Thank you,

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## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No. : 09 / 287,478 Confirmation No. 6350  
Applicant : Christian S. Rode  
Filed : April 6, 1999  
Provisional Appl. Filed : 60 / 080,905, 4/06/98  
TC/A.U. : 2123  
Examiner : Thai Phan  
Docket No. : RCI001v1

Honorable Commissioner for Patents

P.O. Box 1450

Alexandria VA 22313-1450

## INFORMATION DISCLOSURE STATEMENT

"No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing this statement after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in Section 1.56(c) more than three months prior to the filing (11/17/2004) of this information disclosure statement."

Gore, et al (USP 5,278,770) demonstrates the known art of generating customized SPICE input decks from user-specified data.

It would appear that at least claim 1 of Mattos, et al (USP 6,292,766) would apply to the present application,

Claim 1. In a computer system, a simulation tool input file generator, comprising:

a user interface for selecting circuit description files that describe electrical characteristics of interface circuitry in an integrated circuit chip and for entering programmable values associated with said electrical characteristics in said circuit description files, said interface circuitry comprising an input/output buffer circuit and a pad,

a simulation tool input file associated with said interface circuitry, said simulation tool input file comprising a description of said electrical characteristics and said programmable values of said input/output buffer circuit, and said pad, said electrical characteristics and said programmable values compatible with a simulation tool input protocol; and

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a simulation model generator for automatically generating said simulation tool input file corresponding to said interface circuitry on said integrated circuit chip, said simulation model generator generating said simulation tool input file by: first converting said electrical characteristics and programmable values into a file format that is compatible with said simulation tool input file protocol; and second automatically inserting resistances, inductances, capacitances and electrical characteristics required to complete a formulation of said simulation tool input file description of said interface circuitry, wherein said model generator automatically indicates in said simulation tool input file a bus connection between a plurality of said input/output buffer circuits.

The present application has as its prime example signal integrity simulation of components driving transmission lines, including bus-like configurations, and in doing so, generates intermediate simulation tool input files for simulation by SPICE. The system provides for user selection of different drivers or for a generic driver with configurable parasitics. Resistances, inductances and capacitances are part of the generated file, with the only apparent meaningful distinction from the present application being "wherein said model generator automatically indicates in said simulation tool input file a bus connection between a plurality of said input/output buffer circuits." The present application is intended to embrace all types of SPICE circuit and other simulation data within its scope, including bus circuits, although we are unsure what "special indication" would be presented for the purposes of identifying a bus.

It would appear at least claim 1 of 6,530,065 would apply to the present application, although the provisional for 6,530,065 was filed after the regular filing for the present application. Specifically, this patent claims in Claim 1 (and similarly, in claim 4):

Claim 1. A method for simulating a circuit in a client-server environment, wherein a network couples at least one client computer to a server computer, the method comprising:

at the client computer, presenting a visual display, wherein the visual display includes a visual depiction of a particular circuit having two or more components, and wherein at least one of the depicted components is linked to one or more user interface controls for receiving user input to change component characteristic data for the depicted component,

providing executable code to the client computer from the server computer,

at the server computer, generating simulation data that represents one or more characteristics of a signal that would be generated in the particular circuit during operation of the particular circuit,

sending the simulation data over the network from the server computer to the client computer;

at the client computer, generating a first simulation display based on the simulation data for operation of the particular circuit;

receiving user input at the client computer; and

at the client computer and without requesting additional simulation data from the server computer, generating a second simulation display based on the

simulation data, wherein the second simulation display displays the simulation data differently than the first simulation display, and wherein the second simulation display is generated in response to the user input and in response to executing by the client computer the executable code.

In the present invention, the simulation data is sent in the form of plot data, and a second display in response to a user interface change was specifically demonstrated in Fig 4-K. A zoom function is demonstrated using a scaled version of the identical static plot, as well as by making use of Adobe Acrobat as a target plot format (which allows zooming). It was also anticipated that the raw simulation data could be sent to a Java plotting applet for further processing, as had been widely done in many applications before the filing date of 6,530,065.



PTOSB:7 (10-04-02)

Approved for use through 10/21/2005. OAO 0001-0000

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# FEE TRANSMITTAL

## for FY 2005

Effective 10/01/2004. Patent fees are subject to annual revision.

☒ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT (\$) 180

## Complete if Known

Application Number 09/267,478

Filing Date April 5, 1999

First Named Inventor Christian S. Rode

Examiner Name Eric Q. Phelan

Art Unit 2128

Attorney/Agent No. RCI061v1

## METHOD OF PAYMENT (check all that apply)

☐ Check ☒ Credit card ☐ Money ☐ Other ☐ None☐ Deposit Account

Deposit Account Number

Deposit Account Name

The Director is authorized to: (check all that apply)

☒ Charge fee(s) indicated below ☐ Credit any overpayments☐ Charge any additional fee(s) or any underpayment of fee(s)☐ Charge fee(s) indicated below, except for the filing fee

to the above-described deposit account.

## FEE CALCULATION

1. BASIC FILING FEE

Large Entity Small Entity

Fee Code (\$) Fee Code (\$)

1001 140 2001 355

1002 350 2002 175

1003 350 2003 275

1004 750 2004 395

1005 160 2005 80

SUBTOTAL (1) (\$) 80

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

Total Claims Independent Claims Multiple Dependent

20\*\* 3\*\* X

1007 150 1007 150

1008 150 1008 150

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## FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Small Entity

Fee Code (\$) Fee Code (\$)

1001 130 2001 65

1002 30 2002 25

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1008 130 2008 130

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